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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/835,132	03/30/2001	Balaji Parthasarathy	219.39505X00-P10751	4226

7590 05/19/2004

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/835,132	PARTHASARATHY ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8-12,19 and 20* is/are rejected.

7)☒ Claim(s) *2-7 and 13-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

3. Claims 11 and 20 rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 11 and 20 both contain a trademark (InfiBand ™) used as a claim limitation. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. A claim which uses a trademark or trade name as a limitation to identify or describe a particular material or product does not comply with the requirements of 35 USC § 112 2nd paragraph. *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. In fact, the value of a trademark would be lost to the extent that it became descriptive of a product, rather than used as an identification of a source or origin of a product. Thus, the use of a trademark or trade name in a claim to identify or describe a material or product would not only render a claim indefinite, but would also constitute an improper use of the trademark or trade name.

3.1. The following terms lack proper antecedent basis:

3.1.1. "said ME instruction" (claim 9 line 5);

3.1.2. "the host interface" (claim 9, lines 8 and 11);

3.1.3. "the address translation interface" (claim 9, lines 8 and 12; claim 19 lines 8 and 12);

3.1.4. "the context memory interface" (claim 9, lines 9 and 12);

3.1.5. "the local bus interface" (claim 9, lines 9 and 12; claim 19 lines 9 and 12);

3.1.6. "the completion queue/doorbell manager" (claim 9, lines 9 and 13; claim 19 lines 9 and 13); and,

3.1.7. "and the FIFO interface" (claim 9, lines 10 and 13, claim 19 lines 10 and 13).

4. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 8-12, and 19-20 are rejected under 35 USC § 102(b) as being clearly anticipated by Gaddis et al., U.S. Patent 5,457,681.

Gaddis et al. taught (e.g. see figs. 1-17) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

5.1. a host-fabric adapter (fig. 12) comprising;

5.2. at least one Micro-Engine (ME) ("CONTROL MICROPROCESSOR) arranged to establish connections and support data transfers, via a switched fabric ("ATM"), in response to work requests from a host system for data transfers (hosts are attached to ethernet segments 1-n);

5.3. interface blocks ("ATM CELL PROCESSOR", "ETHERNET CONTROLLER") arranged to interface said switched fabric and said host system, and send/receive work requests and/or data for data transfers, via said switched fabric, and configured to provide context information ("ROM", "RAM") needed for said Micro-Engine (ME) to process said work requests for data transfers, via said switched fabric;

5.4. wherein said Micro-Engine (ME) is implemented with a pipelined instruction execution architecture to handle one or more ME instructions and/or one or more tasks so as to process data for data transfers (col. 5 lines 5-9).

6. As to claim 8, Gaddis et al. taught a serial interface ("ATM CELL PROCESSOR") arranged to receive and transmit data from said switched fabric for data transfers, a host interface arranged to receive and transmit work requests, in the form of work queue elements (WQEs), from said host system for data transfers ("SERIAL INTERFACE ADAPTER"), a context memory arranged to store context information needed for said Micro-Engine (ME) to process work requests for data transfers ("RAM"), a first-in/first-out (FIFO) interface

arranged to receive data from said switched fabric via said serial interface, and to transmit data to said switched fabric via said serial interface ("DUAL-PORTED SHARED MEMORY"), an address translation interface arranged for address translation from said Micro_engine (ME) (a component of the 80486 or MC68030 used as the "CONTROL MICROPROCESSOR"), a local bus interface arranged to support system accessible context connections and data transfers (32), and a completion/queue/doorbell manager interface arranged to provide an interface to completion queues, and to update the context information needed for said Micro-Engine (ME) to process work requests for data transfers (figs. 11, 15, 17).

7. As to claim 9, Gaddis et al. taught one or more Data Multiplexers arranged to supply appropriate interface data based on an ME instruction ("DUAL-PORTED SHARED MEMORY", "ETHERNET CONTROLLER"), an instruction memory arranged to provide said ME instruction based on downloadable MicroCode ("RAM"), an Arithmetic Logic Unit (ALU) arranged to perform mathematical, logical and shifting operations, and supply write data to the host interface, the address translation interface, the context memory interface, the local bus interface, the completion queue/doorbell manager interface, and the FIFO interface, via a system data bus (an ALU is present inside both the 80486 and MC68030 CPU's), an Instruction Decoder arranged to supply system controls to the host interface the address translation interface, the context memory interface, the local bus interface, the completion queue/doorbell manager interface, and the FIFO interface, via a system control bus, to execute said ME instruction from said Instruction Memory to control operations of said Data Multiplexers, and to determine functions of said Arithmetic Logic Unit (ALU) (an instruction decoder is also present inside both the 80486 and MC68030 CPU's).

8. As to claim 10, Gaddis et al. taught that the Instruction Memory corresponds to a random-access-memory (RAM) provided to store Microcode that are downloadable for providing said ME instruction to said Instruction Decoder ("RAM").

9. As to claim 11, Gaddis et al. taught that the interface blocks were configured in accordance with an interface specification (ATM), and were implemented as part of an

Application Specific Integrated Circuit (ASIC) (col. 5 lines 15-19).

10. As to claims 12, and 19-20, they do not teach or define above the invention claimed in claims 1, 9, and 11 and are therefore rejected under Gaddis et al. for the same reasons set fourth in the rejection of claims 1, 9, and 11, supra.

11. Claims 2-7 and 13-18 are objected to as being dependent upon a rejected base claim, but would render the base claim allowable if bodily incorporated into the base claim such that the new base claim included all of the original limitations of the base claim, any intervening claims, and the objected claim.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 5,720,032 discloses a network switching system which also operates with a pipeline architecture. US Patent Application Publication 2002/0,126,705 discloses a network traffic routing processor which also operates with a pipeline structure.

13. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
May 13, 2004

RICHARD L. ELLIS
PRIMARY EXAMINER